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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/984,563	12/03/1997	JEFFREY S. MAILLOUX	95-0653.03	2304

21186 7590 07/16/2007

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ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
07/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 08/984,563
Filing Date: December 03, 1997
Appellant(s): MAILLOUX ET AL.

Mark V. Muller
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/11/2007 appealing from the Office action mailed 3/30/07.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

A statement identifying related appeals and interferences in the brief is correct (see below).

"A first, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,561 (Atty. Ref. No. 303.623US6). However, a Notice of Allowance indicating allowance of all claims was subsequently mailed to the Appellant, and the application has now issued as U.S. Pat. No. 6,615,325. This matter never appeared before the Board.

A second, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,560 (Atty. Ref. No. 303.623US2). The Board issued a decision in this matter, allowing all claims (Appeal 2004-0414, attached hereto), and the application has now issued as U.S. Pat. No. 7,103,742. This matter is no longer before the Board.

A third, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,701 (Atty. Ref. No. 303.623US5). The Board issued a decision in this matter, allowing all claims (Appeal 2004-1705, attached hereto). The application has not yet

issued, and is no longer before the Board.

A fourth, related appeal was filed with respect to U.S. Patent Application serial Number 08/984,562 (Atty. Ref. No. 303.623US3). The Board issued a decision in this matter, allowing all claims except claim number 61 (Appeal 2005-1725, attached hereto), and the application has now issued as U.S. Pat. No. 7,124,256. This matter is no longer before the Board.

A fifth, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,560 (Atty. Ref. No. 303.623US1). However, prosecution has been reopened by the Office in this matter, and it was never pending before the Board.

There are no other appeals, interferences, or judicial proceedings known to Appellant that will have a bearing on the Board's decision in the present appeal."

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5610864	Manning	5-1997
6065092	Roy	5-2000
5293347	Ogawa	3-1994

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 59-62 and 68-69 are rejected under 35 U.S.C. 103(a).

Claims 59-62 and 68-69 are rejected under 35 U.S.C. 103(a) as obvious over by Manning, U.S. Patent 5,610,864 in view of Roy U.S. Patent No. 6,065,092 or Ogawa U.S. Patent 5,293,347.

As to claim 59, *Manning* discloses a method of accessing a memory (Fig. 1), comprising: receiving an external row address (Fig. 1 and Fig. 2, ADDR, ROW);

choosing whether the memory is in a burst mode of operation (col. 6 lines 14-26 and col. 7 lines 40-55) or in a standard mode, page mode or standard fast page mode of operation (col. 6 lines 14-26 and col. 7 lines 40-55); selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); and executing a read or write operation (Fig. 2, /WE). Manning further discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55). In other words, since the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed and switching between the various modes is possible, one of ordinary skill in the memory art would have concluded that Manning teaches claimed limitation of choosing between a burst or a pipeline mode of operation.

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory

selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory selectively operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one

of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory selectively operable in a pipeline mode of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Alternatively, Ogawa discloses the memory selectively operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by

providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 60, *Manning* further discloses a burst mode (col. 6 lines 14-26 & col. 7 lines 43-54 and Fig. 1). *Roy* further discloses the pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62). *Ogawa* further discloses the pipeline mode (abstract and col. 4 lines 9-12, 57-61,& col. 22+).

As to claims 61, *Manning* further discloses switching between a read and a write operations (Fig. 2 /WE). *Ogawa* further discloses switching between a read and a write operations (Fig. 1 /WE).

As to claim 62, *Manning* further discloses the operations are performed in a different order (Fig. 1 Ref. 40 and col. 5 lines 43-49, col. 4 lines 23+, & col.6 lines 14+, switching between reads on this limitation).

As to claim 68, *Manning* discloses a method for data transfer direction selection in a memory (Fig. 1), comprising: selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); selecting a burst (col. 6 lines 14-26 and col. 7 lines 40-55) or a standard mode, page mode or standard fast page mode of operation (col. 6 lines 14-23 and col. 7 lines 40-55) for the memory and selecting an external address only path, obtaining external address when

the page mode operation is selected (by definition of a page mode, since a new external column address is provided every CAS cycle in the page mode, col. 1 lines 32-36); and selecting an initial buffered external address data path, obtaining an initial external column address, accessing the memory, and generating internal column address when the burst mode operation is selected (by definition of a burst mode, col. 5 lines 50-57). Manning further discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55). In other words, since the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed and selecting between the various modes is possible, one of ordinary skill in the memory art would have concluded that Manning teaches selecting a burst or a pipeline mode of operation.

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory

selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory selectively operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one

of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory selectively operable in a pipeline mode of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Alternatively, Ogawa discloses the memory selectively operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by

providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 69, *Manning* discloses a storage device (Fig. 1), comprising: mode circuitry configured select between a burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a standard mode, page mode or standard fast page mode of operation (col. 6 lines 14-26 and col. 7 lines 40-55); selection circuitry for selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); an external column address data path for page read and write operation column address retrieval (by definition of a page mode, since a new external column address is provided every CAS cycle in the page mode, col. 1 lines 32-36), an internal column address generation module for burst read and write operation column address generation (by definition of a burst mode, col. 5 lines 50-57); and page/burst circuitry coupled to the mode selection circuitry and configured to switch between page mode and the burst mode for operating the storage device in either mode (col. 6 lines 14-26 and col. 7 lines 40-55).

Manning further discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning)

and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), In other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed and selecting between the various modes is possible, one of ordinary skill in the memory art would have concluded that Manning teaches mode circuitry configured select between a burst mode and a pipeline mode of operation

.However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory selectively operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory selectively operable in a pipeline mode of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Alternatively, Ogawa discloses the memory selectively operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

(10) Response to Argument

Response to argument regarding the rejection of claims 59-62 and 68-69 under 35 U.S.C. 103(a).

A. Appellants' argument on pages 9-11 in the Appeal Brief that "the combination of references does not teach all limitations" has been fully considered but it is not persuasive.

First of all, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "true pipelined operation, with column-based switching in addition to row-based switching" and "switching between burst and pipelined modes on the fly") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Manning discloses choosing whether the memory is in a burst mode of operation (col. 6 lines 14-26 and col. 7 lines 40-55) or a standard mode, page mode or standard fast page mode of operation (col. 6 lines 14-26 and col. 7 lines 40-55); selecting a burst (col. 6 lines 14-26 and col. 7 lines 40-55) or a standard mode, page mode or standard fast page mode of operation (col. 6 lines 14-26 and col. 7 lines 40-55); and mode circuitry configured select between a burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a standard mode, page mode or standard fast page mode of operation (col. 6 lines 14-26 and col. 7 lines 40-55). Manning further discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55). In other words, since the

pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed and switching between the various modes is possible, one of ordinary skill in the memory art would have concluded that Manning further teaches claimed limitation of choosing between a burst or a pipeline mode of operation. .

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory selectively operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the

purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory selectively operable in a pipeline mode of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Alternatively, Ogawa discloses the memory selectively operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Therefore, the combination of references discloses all limitations.

B. Appellants' argument on pages 12-13 in the Appeal Brief that "No motivation to combine the references" and "No reasonable expectation of success" has been fully considered but it is not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in

the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, *Manning* discloses choosing whether the memory is in burst (col. 6 lines 14-26 and col. 7 lines 40-55) or a standard mode, page mode or standard fast page mode of operation (col. 6 lines 14-26 and col. 7 lines 40-55); selecting a burst (col. 6 lines 14-26 and col. 7 lines 40-55) or a page mode of operation (col. 6 lines 14-21 and col. 7 lines 40-55); and mode circuitry configured select between a burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a page mode of operation (col. 6 lines 14-26 and col. 7 lines 40-55). Manning further discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55). In other words, since the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed and switching between the various modes is possible, one of ordinary skill in the memory art would have concluded that Manning further teaches claimed limitation of choosing between a burst or a pipeline mode of operation. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read,

memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory selectively operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory

access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory selectively operable in a pipeline mode of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Alternatively, Ogawa discloses the memory selectively operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline

mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Therefore, the references discloses motivation to combine the references and reasonable expectation of success.

(11) Related Proceeding(s) Appendix

Copies of the court or Board decision(s) identified in the Related Appeals and Interferences section of this examiner's answer are provided herein.

Copies of the decisions in related appeals are 2004-0414, 2004-1705, and 2005-1725.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/HONG CHONG KIM/
PRIMARY EXAMINER

Hong Kim

Conferees:

Lynne Browne
APPEAL PRACTICE SPECIALIST, TQAS
TECHNOLOGY CENTER 2100

Sanjiv Shah

/Sanjiv Shah/
SANJIV SHAH
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TECHNOLOGY CENTER 2100

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board

Paper No. 37

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte JEFFEREY S. MAILLOUX, KEVIN J. RYAN, TODD A. MERRITT, AND BRETT L. WILLIAMS

Appeal No. 2004-0414
Application 08/984,560

ON BRIEF

MAILED
OCT 28 2004
U.S. PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

Schwegman, Lundberg
Woessner & Kluth, P.A.
NUV 0 2 2004
CMG RECEIVED

Before THOMAS, BARRY and LEVY, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 11-21 and 59-71.

Representative claim 11 is reproduced below:

11. A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing schemes and said patterned addressing scheme is selected.

The following reference is relied on by the examiner:

Manning	5,610,864	Mar. 11, 1997 (filing date Feb. 10, 1995)

Claims 11-21 and 59-71 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Manning. Appellant argues and the examiner makes reference at various portions of the answer to an inadvertent reliance upon 35 U.S.C. § 102(b) as the basis to reject the claims on appeal rather than upon 35 U.S.C. § 102(e). To expedite our consideration of the issues on this appeal, we consider the rejection in the same manner.

Rather than repeat the positions of the appellants and the examiner, reference is made to the brief and reply brief for appellants' positions, and to the answer for the examiner's positions.

OPINION

We reverse.

Each of independent claims 11, 59, 60, 61, 62, 65, 68 and 70 variously recite control logic for selecting between a patternless addressing scheme and a patterned addressing scheme

or selecting between a burst or a pipelined mode or selecting between an unpatterned pipelined and a patterned burst data pattern mode of operation. Correspondingly, each of these independent claims also requires the feature of switching circuitry which performs the switching of respective first and second pathways depending on which of the earlier recited addressing schemes is selected.

It goes without saying that those independent claims (59, 60, 61 and 70) that recite specifically selecting between a pipelined or a burst mode of operation are the most specific claims. On the other hand, the remaining independent claims (claims 11, 62, 65 and 68) more broadly recite the same features in a corresponding manner as to patternless and patterned addressing schemes. It is noted that the discussion at specification page 30 beginning at line 5 and at specification page 33 beginning at line 13 clearly indicates to the artisan that a patternless addressing scheme is only taught in the context of a pipelined mode of operation and that a patterned addressing scheme is only taught in a corresponding burst mode of operation.

With these considerations in mind, our study of Manning leads us to agree with appellant's assessment of this reference generally set forth in the paragraph bridging pages 3 and 4 of the principal brief on appeal. The examiner's position primarily relies upon Manning's Figure 1 as well as portions of columns 5-7. Column 5, lines 43-46 merely indicates that pipelined architectures exist as other types of memory architectures that may be applicable to the current disclosure in Manning, yet no details are supplied in any other portion of the reference to suggest the specific applicability of the burst mode operability of Manning's memory to a pipelined architecture, specifically as to how it would be implemented. The teachings at column 5, lines 43-62, in context, merely appear to teach the conceptual applicability of burst mode architectures to pipelined architectures but not presenting any further circuits in the remaining parts of the specification of Manning applicable to pipelined architectures.

Various modes are taught at column 6, lines 14-34 and column 7, lines 29-54 as relied upon by the examiner. These various modes, however, do not teach any switchability between a burst mode and a pipelined mode of operation as required by each of the

claims on appeal. We therefore agree with appellant's observation at the top of page 7 of the principal brief on appeal that "Manning never discusses the ability to switch or select between burst and pipelined modes of operation, or patternless and patterned addressing schemes, as claimed by the Appellants."

In order for us to sustain the examiner's rejection under 35 U.S.C. § 103, we would need to resort to speculation or unfounded assumptions to supply deficiencies in the factual basis of the rejections. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968), reh'g denied, 390 U.S. 1000 (1968). This we decline to do.

Our reviewing court has made it clear in In re Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), and In re Zurko, 111 F.3d 887, 42 USPQ2d 1476 (Fed. Cir. 1997), that rejections must be supported by substantial evidence in the administrative record and that where the record is lacking in evidence, this Board cannot and should not resort to unsupported speculation. As indicated in Lee, 277 F.3d at 1343-44, 61 USPQ2d at 1433-34, the examiner's finding of whether there is a teaching, motivation or suggestion to combine the teachings of the applied references must not be resolved based on "subjective belief and unknown authority," but must be "based on objective evidence of record."

The examiner's responsive arguments portion of the answer beginning at page 5 merely repeats the initial reliance in the

statement of the rejection on certain portions of columns 5-7 of Manning. As indicated earlier, these portions of Manning clearly fall short of indicating to us the anticipatory nature of the subject matter of the claims on appeal at least as applied to pipelined memory schemes. Plainly, Manning does not explain and certainly does not show in Figure 1 of his patent switching circuitry to switch between plural pathways between a pipelined/patternless addressing scheme and a burst/patterned addressing scheme, which is the essential argument provided in the brief and reply brief by appellants. More specifically, Manning does not further develop the general statement of applicability at columns 5, lines 43-46 of his invention being usable with pipelined architectures such as to explain how a plurality of memory-type operations may occur in an overlapping manner or processed simultaneously in a manner consistent in the art and recognized to be necessary for a pipelined memory accessing scheme.

Therefore, Manning alone, within 35 U.S.C. 102(b) or § 102(e), without additional evidence, cannot be fairly said to anticipate the subject matter of each independent claim on appeal. As such, the rejection of the respective dependent claims must be reversed as well.

In view of the foregoing, the decision of the examiner rejecting all claims on appeal under 35 U.S.C. § 102 is reversed.

REVERSED

James D. Thomas)
Administrative Patent Judge)
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)
Lance Leonard Barry) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
) INTERFERENCES
)
)
Stuart S. Levy)
Administrative Patent Judge)

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The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board

Paper No. 42

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

MAILED
FEB 25 2005
U.S. PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JEFFREY S. MAILLOUX,
KEVIN J. RYAN,
TODD A. MERRITT
and
BRETT L. WILLIAMS

Appeal No. 2004-1705
Application 08/984,701

HEARD: February 8, 2005

Before THOMAS, BARRY and LEVY, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 40-43, 45, 59, 60, 62-87. At pages 2 and 4 of the answer, the examiner withdrew the rejection of claims 64, 67, 68, 73-75

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and 83-85 under 35 U.S.C. § 102(a), and the separate rejection of all claims on appeal under 35 U.S.C. § 103. Only the rejection of claims 40-43, 45, 59, 60, 62, 63, 65, 66, 69-72, 76-82, 86 and 87 remain for our consideration.

Representative claim 43 is reproduced below:

43. A memory module comprising:

a plurality of memories of which at least one of said memories includes a mode select pin for switching as between a burst mode and a pipelined mode of operation.

The following reference relied on by the examiner is:

Manning	5,610,864	Mar. 11, 1997 (filing date Feb. 10, 1995)

Claims 40-43, 45, 59, 60, 62, 63, 65, 66, 69-72, 76-82, 86 and 87 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Manning.

Rather than repeat the positions of the appellants and the examiner, reference is made to the brief and reply brief for the appellants' positions, and to the answer for the examiner's positions.

OPINION

We reverse.

Each of independent claims 40, 43, 59, 60, 63, 65, 66, 69, 77, 81 and 86 variously recite in some manner a mode select pin for switching between a burst mode and a pipelined mode of operation.

Our study of Manning leads us to agree with appellants' assessment of this reference generally set forth at pages 5-8 of the principal brief on appeal. The examiner's position primarily relies upon Manning's Figure 1 as well as portions of columns 5-7. Column 5, lines 43-46 merely indicates that pipelined architectures exist as other types of memory architectures that may be applicable to the current disclosure in Manning, yet no details are supplied in any other portion of the reference to suggest the specific applicability of the burst mode operability of Manning's memory to a pipelined architecture, specifically as to how it would be implemented. The teachings at column 5, lines 43-62, in context, merely appear to teach the conceptual applicability (the possibility in appellants' words) of burst mode architectures to pipelined architectures but not presenting any

further circuits in the remaining parts of the specification of Manning applicable to pipelined architectures.

Various modes are taught at column 6, lines 14-34 and column 7, lines 29-54 as relied upon by the examiner. The various modes, however, do not teach any switchability between a burst mode and a pipelined mode of operation as required by each of the claims on appeal. We therefore agree with appellants' observation at page 8 of the principal brief on appeal that "Col. 5, lines 41-50 discusses the possibility of using a pipelined architecture, but not as enabling switching between pipeline or burst operations within the same memory, as disclosed and claimed by the Appellants."

In order for us to sustain the examiner's rejection over prior art, we would need to resort to speculation or unfounded assumptions to supply deficiencies in the factual basis of the rejections. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968), reh'g denied, 390 U.S. 1000 (1968). This we decline to do.

Our reviewing court has made it clear in In re Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), and In re Zurko, 111 F.3d 887, 42 USPQ2d 1476 (Fed. Cir. 1997), that rejections must be supported by substantial evidence in the administrative record and that where the record is lacking in evidence, this Board cannot and should not resort to unsupported speculation. As indicated in Lee, 277 F.3d at 1343-44, 61 USPQ2d at 1433-34, the examiner's positions must not be resolved based on "subjective belief and unknown authority," but must be "based on objective evidence of record."

The examiner's responsive arguments portion of the answer beginning at the fourth page merely repeats the initial reliance in the statement of the rejection on certain portions of columns 5-7 of Manning. As indicated earlier, these portions of Manning clearly fall short of indicating to us the anticipatory nature of the subject matter of the claims on appeal at least as applied to pipelined memory schemes. Plainly, Manning does not explain and certainly does not show in Figure 1 of his patent switching circuitry to switch between a pipelined mode addressing

scheme and a burst mode addressing scheme, which is the essential argument provided in the brief and reply brief by appellants. More specifically, Manning does not further develop the general statement of applicability at column 5, lines 43-46 of his invention being usable with pipelined architectures such as to explain how a plurality of memory-type operations may occur in an overlapping manner or processed simultaneously in a manner consistent in the art and recognized to be necessary for a pipelined memory accessing scheme.

Therefore, Manning alone, within 35 U.S.C. § 102(a), without additional evidence, cannot be fairly said to anticipate the subject matter of each independent claim on appeal. As such, the rejection of the respective dependent claims must be reversed as well.

In view of the foregoing, the decision of the examiner rejecting all claims on appeal under 35 U.S.C. 102 is reversed.

REVERSED

James D. Thomas
Administrative Patent Judge)
)
)
) BOARD OF PATENT
Lance Leonard Barry) APPEALS AND
Administrative Patent Judge) INTERFERENCES
)
)
)
Stuart S. Levy)
Administrative Patent Judge)

JDT/cam

Appeal No. 2004-1705
Application No. 08/984,701

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The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

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U.S. PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JEFFREY S. MAILLOUX, KEVIN J. RYAN,
TODD A. MERRITT, and BRETT L. WILLIAMS

Appeal No. 2005-1725
Application No. 08/984,562

HEARD: October 19, 2005

Before DIXON, GROSS, and BLANKENSHIP, ***Administrative Patent Judges.***

GROSS, ***Administrative Patent Judge.***

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DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 22 through 32, 59, 61, 63, and 66 through 72, which are all of the claims pending in this application.

Appellants' invention relates to a memory device that selectively operates in either burst or pipelined modes. Claim 22 is illustrative of the claimed invention, and it reads as follows:

22. A memory circuit, comprising:

control logic for providing a selected mode control signal;

Schwegman, Lundberg,
Woessner & Kluth, P.A.

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selection and temporary storage circuitry for receiving and storing a first external address; and

a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching the memory circuit between a burst mode and a pipelined mode.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Manning	5,610,864	Mar. 11, 1997 (Filed Feb. 10, 1995)
Manning (Manning II)	5,729,503	Mar. 17, 1998 (Filed Jul. 24, 1995)

Claims 22 through 32, 59, 61, and 66 through 72 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Manning.

Claims 22 through 32, 59, 61, 63, and 66 through 72 stand rejected under 35 U.S.C. § 103 as being unpatentable over Manning II in view of Manning.

Reference is made to the Final Rejection (Paper No. 29, mailed October 23, 2002), the Examiner's Answer (Paper No. 32, mailed June 3, 2003), and the Supplemental Examiner's Answer (Paper No. 37, mailed February 23, 2004) for the examiner's complete reasoning in support of the rejections, and to appellants' Brief (Paper No. 31, filed February 10, 2003), Reply Brief (Paper No. 34, filed August 7, 2003), and Supplemental

Reply Brief (Paper No. 39, filed March 26, 2004) for appellants' arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the anticipation rejection of claims 22 through 32, 59, and 66 through 72 but affirm the anticipation rejection of claim 61. Likewise, we will reverse the obviousness rejection of claims 22 through 32, 59, 63, and 66 through 72 but affirm the obviousness rejection of claim 61.

Regarding the anticipation rejection of independent claims 22, 59, and 66, the examiner (Answer, pages 8 and 10) directs attention to column 6, lines 14-16, and column 7, lines 44-55, for the claimed switching between a burst mode and another mode and to column 5, lines 43-49, for the claimed pipelined mode. The examiner reasons (Answer, pages 8 and 10) that "in order to work in a standard EDO memory including a pipeline architecture, one has to select a pipelined mode if one is in a burst mode." The examiner continues with an explanation as to why it would

have been obvious to include a pipelined architecture in the system of Manning.

Appellants contend (Brief, page 9) that although Manning mentions the possibility of using a pipelined architecture, and discloses switching between burst and standard EDO modes, Manning fails to disclose selecting or switching between burst and pipelined modes of operation. We agree. Manning merely teaches that there may be a pipelined mode or there may be switching between two modes, one of which may be a burst mode. We find nothing in Manning to suggest that the standard EDO mode is, or could be, a pipelined mode of operation. Accordingly, we cannot sustain the anticipation rejection of claims 22, 59, and 66, nor of their dependents, claims 23 through 32 and 67 through 72.

Claim 61 does not require switching or selecting between burst and pipeline modes. Instead, the switching in claim 61 is merely between two modes of operation, which could include Manning's burst and standard EDO modes. However, claim 61 also recites that control logic provides "an internal mode control signal." Appellants' sole argument for claim 61 (Brief, pages 7 and 8) is that Manning only uses an external mode control signal. However, appellants fail to point to anything in the reference that would suggest an external mode control signal rather than an

internal mode control signal. Attorney argument cannot take the place of evidence in the record. ***Estee Lauder Inc. v. L'Oreal, S.A.***, 129 F.3d 588, 595, 44 USPQ2d 1610, 1615 (Fed. Cir. 1997). Therefore, we find appellants' argument unpersuasive, and we will affirm the anticipation rejection of claim 61 over Manning.

For the obviousness rejection of claims 22 through 32, 59, and 66 through 72, the examiner applies Manning II in view of Manning. The examiner acknowledges (Final Rejection, pages 6-7) that Manning II discloses switching between a burst mode and a page mode rather than between a burst mode and a pipelined mode, as recited in independent claims 22, 59, and 66. In fact, Manning II fails to disclose a pipelined mode at all. The examiner, however, asserts (Final Rejection, page 7) that

> it was well known in the memory art . . . to use the pipeline mode to access memory per each cycle thereby increasing the access speed. For example, Manning (864) discloses a pipelined mode (col. 5 lines 43-50) for he [sic] purpose of increasing the throughput by accessing data per every cycle (col 5 lines 46-48) thereby increasing the system throughput.

The examiner concludes that it would have been obvious to "modify a page mode of 503 with a pipelined mode of 864 because it would increase the throughput by accessing data per every cycle thereby increasing the system throughput."

Appellants argue (Brief, page 10) that Manning fails to disclose switching between burst and pipelined modes. Although Manning discusses the possibility of using a pipelined structure, appellants explain (Brief, page 10), Manning provides no details as to how the use of a pipelined structure might be accomplished. We agree with appellants. Manning's suggestion to use a pipelined structure is insufficient to suggest switching between burst and pipelined modes. As indicated ***supra***, we find nothing in Manning to suggest substituting a pipelined mode for the standard EDO such that selecting or switching between burst and pipelined modes can occur. Accordingly, we cannot sustain the obviousness rejection of claims 22, 59, and 66, nor of their dependents, claims 23 through 32 and 67 through 72.

Regarding claim 63, the "wherein" clause at the end of the claim appears to be incorrect. We believe that the claim should end with "when the selected mode control signal indicates a ***burst*** mode" (emphasis ours). We are treating this as an obvious informality that was acknowledged at the oral hearing on October 19, 2005. As such, claim 63 recites that the mode control signal selects either a pipeline mode or a burst mode. As we indicated ***supra***, we find no disclosure in either Manning or Manning II to

suggest selecting between burst and pipelined modes of operation. Accordingly, we cannot sustain the rejection of claim 63.

As to claim 61, appellants' sole argument (Brief, pages 13 and 16) is that neither Manning nor Manning II discloses an internal mode control signal without pointing to any evidence supporting appellants' assertion. Without any supporting evidence, appellants' assertion is insufficient to overcome the prima facie case of obviousness presented by the examiner. Accordingly, we will affirm the obviousness rejection of claim 61.

CONCLUSION

The decision of the examiner rejecting claims 22 through 32, 59, and 66 through 72 under 35 U.S.C. § 102 and claims 22 through 32, 59, 63, and 66 through 72 under 35 U.S.C. § 103 is reversed. However, the decision of the examiner rejecting claim 61 under 35 U.S.C. §§ 102 and 103 is affirmed. Accordingly, the examiner's decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

JOSEPH L. DIXON
Administrative Patent Judge

ANITA PELLMAN GROSS
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

APG/vsh

Appeal No. 2005-1725
Application No. 08/984,562

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